REMARKS

I. Status Of Claims

Claims 1-16 are pending in the present application. Claims 1, 6, 9, 11, and 14 are amended herein. Claims 3 and 7 are canceled. New Claims 17 and 18 have been added. Therefore, upon entry of this Amendment, Claims 1, 2, 4-6, and 8-18 will be pending. No new matter has been introduced by the present amendment. Reconsideration of the application as amended and based on the arguments set forth hereinbelow is respectfully requested.

II. Claim Rejections Under 35 U.S.C. §102

Claims 1, 2, and 10-15 stand rejected by the Examiner under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,953,276 to Baker (hereinafter, "Baker"). This rejection is respectfully traversed.

Claim 1 recites a converter stage for converting a differential logic input signal and a corresponding common mode differential logic signal each having a first single-ended logic signal and a complementary second single-ended logic signal to a single-ended logic output signal. An example of a converter stage recited by Claim 1 is described with respect to converter stage shown in Figure 4 of the present application. Referring to Claim 1, the recited converter stage includes a first differential stage (such as first differential stage **10** shown in Figure 4) having a first PMOS transistor (such as first PMOS transistor **8** shown in Figure 4) and a second PMOS transistor (such as second PMOS transistor **9** shown in Figure 4). A gate terminal of the first PMOS

transistor is coupled to the first single-ended signal (such as first single-ended signal **5-1** shown in Figure 4) of the common mode level differential signal (such as common mode level differential signal **5** shown in Figure 4). In addition, a gate terminal of the second PMOS transistor is coupled to the second single-ended signal (such as second single-ended signal **5-2** shown in Figure 4) of the common mode level differential signal (such as common mode differential signal **5**). Further, source terminals of the PMOS transistors (such as PMOS transistors **8** and **9**) are connected to a first current source (such as first current source **7** shown in Figure 4). The converter stage recited by Claim 1 also includes a second differential stage (such as second differential stage **11** shown in Figure 4) having a first NMOS transistor and a second NMOS transistor (such as first and second NMOS transistors **13** and **14**, respectively, shown in Figure 4). A gate terminal of the first NMOS transistor (such as NMOS transistor **13**) is coupled to the first single-ended signal (such as first single-ended signal **2-1** shown in Figure 4) of the differential input signal (such as differential input signal **2** shown in Figure 4). A gate terminal of the second NMOS transistor (such as second NMOS transistor **14**) is coupled to the second single-ended signal (such as second single-ended signal **2-2** shown in Figure 4) of the differential input signal (such as differential input signal **2**). In addition, source terminals of the NMOS transistors (NMOS transistors **13** and **14**) are connected to a second current source (such as second current source **12** shown in Figure 4). Drain terminals of the NMOS transistors (NMOS transistors **13** and **14**) are connected to the drain terminals of the PMOS transistors (PMOS transistors **8** and **9**).

The converter stage recited by Claim 1 also includes an output connected to the source terminal of the second PMOS transistor and to the drain terminal of the second NMOS transistor for providing the single-ended output signal. The current sources are controlled by a voltage level that is centered between the mid-potentials of the common mode level differential logic signal and the mid-potential of the differential logic input signal such that both current sources deliver the same constant current.

Summarily, Baker does not teach a converter stage coupled to first and second single-ended signals of a common mode level differential signal and coupled to first and second single-ended signals of a differential input signal, as recited by Claim 1.

The Examiner contends that Figure 3 of Baker teaches all of the features recited by Claim 1. Referring to Figure 3, Baker is directed to a differential amplifier **60** for receiving complimentary input signals +Vin and –Vin on respective complimentary input terminals **62** and **64**, respectively. (Baker, column 4, lines 52-54.) Complimentary output signals +Vout and –Vout are generated on respective complimentary output terminals **66** and **68**. (Baker, column 4, lines 55 and 56.) The Examiner contends that input signals +Vin and –Vin of Baker correspond to the first single-ended signal and the second single-ended signal, respectively, of the common mode level differential signal recited by Claim 1. However, nowhere does Baker teach other inputs, particularly the single-ended signals of the differential input signal, as recited by Claim 1. Rather, Baker merely teaches two input signals (+Vin and –Vin). There is no teaching in Baker of four single-ended signals, as required by Claim 1. Thus, Baker as noted above fails to teach a converter stage coupled to first and second single-ended signals of a common mode

level differential signal and coupled to first and second single-ended signals of a differential input signal, as required by Claim 1.

Further, Baker also does not teach the features recited by element (d) of Claim 1. Because Baker does not teach a common mode level differential signal, Baker cannot teach current sources controlled by a voltage level that is centered between the mid-potential of a differential logic input signal, as recited by element (d) of Claim 1. In addition, Baker does not teach the conversion of a differential logic signal in conjunction with its common mode differential logic signal into a single-ended logic output signal, as required by Claim 1. For these reasons, it is respectfully submitted that Baker does not teach each and every feature recited by Claim 1. In addition, applicants respectfully request that the rejection of Claim 1 under 35 U.S.C. § 102(b) be withdrawn and the claim allowed at this time.

Claims 3 and 7 have been canceled. Claims 2, 4-6, and 8-16 depend from Claim 1. Therefore, the comments presented above relating to Claim 1 apply equally to Claims 2, 4-6, and 8-16. Applicants, therefore, respectfully request that the rejection of Claims 2, 4-6, and 8-16 under 35 U.S.C. § 102(b) be withdrawn and the claims allowed at this time.

III. Allowable Subject Matter

The Examiner objected to Claims 3-9 and 16 as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. (Official Action, page 4.)

Original Claim 3 depended from Claim 2, which depends from base Claim 1. Claim 3 has been canceled. New Claim 17 has been added to include the features of Claims 1-3. Therefore, it is respectfully submitted that new Claim 17 should be allowed at this time.

Original Claim 7 depended from Claim 2, which depended from base Claim 1. Claim 7 has been canceled. New Claim 18 has been added to include the features of Claims 1, 2, and 7. Therefore, it is respectfully submitted that new Claim 18 should be allowed at this time.

IV. Conclusion

In light of the above amendments and remarks, it is respectfully submitted that the present application is now in proper condition for allowance, and such action is earnestly solicited.

If any minor issues should remain outstanding after the Examiner has had an opportunity to study the Amendment and Remarks, it is respectfully requested that the Examiner telephone the undersigned attorney so that all such matters may be resolved and the application placed in condition for allowance without the necessity for another Action and/or Amendment.

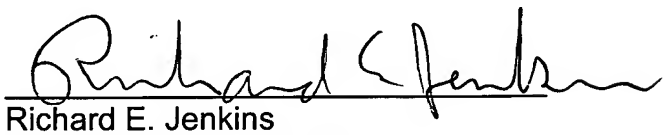
DEPOSIT ACCOUNT

Although it is believed that no fee is due, the Commissioner is hereby authorized to charge any deficiencies of payment associated with the filing of this Response to Deposit Account No. **50-0426**.

Respectfully submitted,

JENKINS, WILSON & TAYLOR, P.A.

Date: January 20, 2005

By: 

Richard E. Jenkins
Registration No. 28,428

REJ/BJO/gwc

Customer No. 25297

1406/168